A High Efficiency GaAs MCM Power Amplifier for 1.9 GHz Digital Cordless Telephones

Satoshi Makioka, Noriyuki Yoshikawa, and Kunihiko Kanazawa

Abstract—**A GaAs MCM power amplifier has been developed for 1.9-GHz digital cordless telephones. Power-added efficiency of 40.2% and $P_{1\,dB}$ of 22.2 dBm have been obtained at drain supply voltage of 3.6 V. Adoption of the multilayer MCM structure, i.e., multilayer microwave integrated circuits (MuMIC), and on-chip ferroelectric capacitors successfully reduced the GaAs total chip area to be 1.1 mm^2. We consider that the MuMIC is the most effective candidate for high frequency circuits.**

I. Introduction

IMPLEMENTATION of a power amplifier in the 1.9-GHz digital cordless telephones is an attractive goal in applying high efficiency GaAs power amplifier IC's. In order to reach this goal, many efforts have been devoted for mainly dealing with linear amplifiers for digital modulation systems (1)–(2). Although GaAs power amplifiers have made considerable progress recently (3)–(6), little achievement has been attained as for increasing efficiency at low drain voltage and reducing the chip area.

The purpose of the present study is to improve these drawbacks by using FET's with low on-resistance and by adopting the multilayer multichip module (MCM) structure and barium strontium titanate (BST) MIM capacitors on the GaAs chips (7). The low on-resistance FET's contribute to achievement of the high efficiency at low drain voltage. The multilayer MCM structure and the BST capacitors result in reducing the GaAs chip area of the power amplifier. We consider that the multilayer MCM structure, which we call the MuMIC, is the most effective candidate for high frequency circuits. This paper describes designing, fabricating, and testing the high efficiency GaAs MuMIC power amplifier for 1.9 GHz Japanese digital cordless telephones.

II. FET Design

The GaAs FET's are used because of advantages of the high efficiency and the low distortion for 1.9 GHz digital cordless telephones. For the purpose of achieving the higher efficiency and the lower voltage operation of 3.6 V, the lightly doped drain (LDD) structure is adopted for the GaAs power FET's. Therefore, the on-resistance is aimed to be lower than 5.2 (Ω)/mm. Fig. 1 shows the cross section of the present FET's. The n-type active layer, the n'-type layer, and the n^+-type contact layer are provided by selective ion-implantation of Si onto an undoped LEC GaAs substrate under the condition of 8×10^{12}-cm^{-2} dose at 50 keV, 1.6×10^{13}-cm^{-2} dose at 50 keV, and 5×10^{13}-cm^{-2} dose at 140 keV, respectively. Au/Ni/AuGe and Al/Ti are used for the Ohmic contacts and the Schottky gate, respectively.

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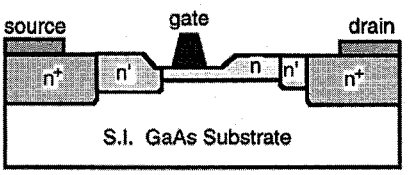


Fig. 1. Cross section of GaAs FET.

TABLE I
Device Geometry of Each Designed FET

	gate length	gate width
1st stage FET	0.6 μm	0.9 mm
2nd stage FET	0.6 μm	0.3 mm
3rd stage FET	0.6 μm	1.0 mm
4th stage FET	0.8 μm	4.2 mm

III. Circuit Design

An equivalent circuit of the power amplifier for the 1.9 GHz digital cordless telephones is shown in Fig. 2. The preamplifier from the first to the third stage is integrated to be one-chip MMIC. The MMIC preamplifier for driving the power MESFET's consist of BST MIM capacitors, bulk resistors on GaAs, and three MESFET's. The first and the second FET's are dual gate FET's for the gain control. The output power of MMIC preamplifiers must be more than 13 dBm, because the MESFET's require an input power of 12.5 dBm to provide the $P_{1\,dB}$ of 22.5 dBm. The 4-stage amplifier circuit is adopted to achieve high gain of over 35 dB. The fourth stage amplifier is composed of a discrete GaAs FET chip and the input and output matching circuits on the surface of the multilayer MCM. The device geometry of each designed FET is shown in Table I.

The main effort has been devoted to the reduction of the GaAs MMIC chip size. Techniques used for reducing the GaAs MMIC chip area are as follows:

1) Adoption of the MCM structure of ceramic multilayer substrate with matching and bias circuits;
2) achievement of the BST MIM capacitors on GaAs chips; and

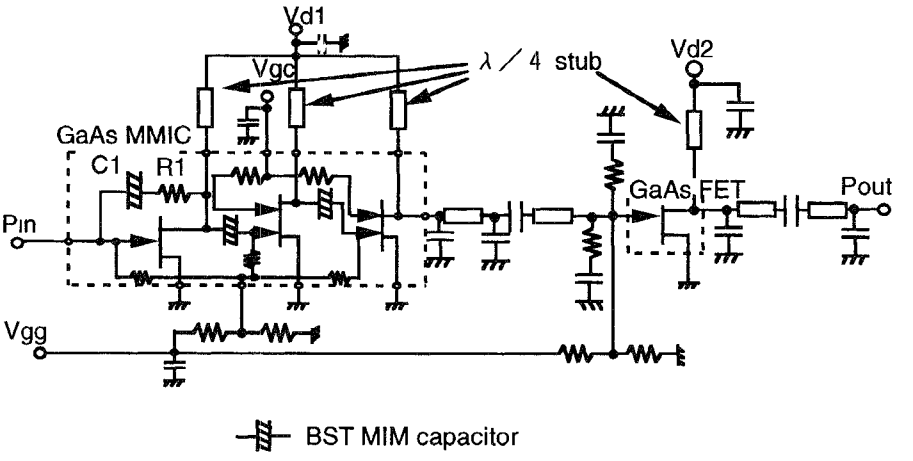


Fig 2 Equivalent circuit of the GaAs power amplifier

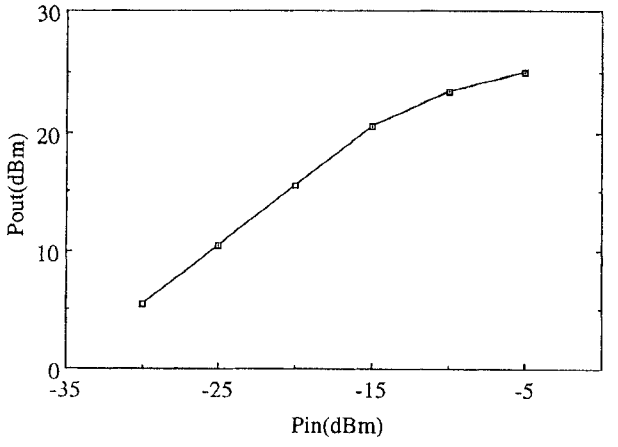


Fig. 3. Simulated input/output characteristics of MuMIC power amplifier.

3) elimination of an input matching circuit by adopting a feedback circuit at the first stage amplifier.

The matching circuits are avoided between the first stage and the second stage, and also between the second stage and the third stage by using large coupling capacitors. This direct connection, that is high impedance matching, circuit degrades the gain of the amplifier. However, the adoption of the large coupling capacitors of 20 pF suppress the loss to be 3.3 dB for each direct connection. These capacitors are provided by on-chip ferroelectric BST capacitors which have large dielectric constant of 300.

The other effort is done for the first stage matching circuit. The feedback circuit composed of R_1 and C_1 as shown in Fig. 2 is adopted for the first stage FET amplifier which uses a 0.9 mm gate width device. These R_1 and C_1 values are designed to be 130 Ω and 20 pF, respectively, in order to offer the 50 Ω input impedance. The simulated input/output impedance characteristics are shown in Fig. 3. The drain current of the first stage FET is designed to be 10mA for providing the high efficiency operation.

Let us now look at the circuit design in detail. We should notice that the gate width of the power FET is important for $\pi/4$-shift QPSK modulation on the point of view of the distortion. The output power, channel leakage power, and

TABLE II
STATZ/RAYTHEON MODEL PARAMETER VALUES

VTO=-2.2V	CGS=4 pF	CDS=0.5pF
β=0.7	CGD=0.4pF	CRF=1100pF
Y=0.01	RG=0 6	RC=500
α=1.5	RD=0.1	IS=1.46e-10 A
B=1	RS=0.1	N=1.480
Vbi=0.553V		Vbr=15 V

power added efficiency of the every stage FET are simulated. We have arrived at the conclution that gate width from the second to the fourth stage FET are designed to be 0.3 mm, 1 mm, and 4.2 mm, respectively. These preamplifiers from the first to the third stage are integrated to be one chip MMIC as shown in Fig. 2.

We carried out the circuit simulation of the large signal operation of the amplifier by using the Raytheon/Statz FET model. The parameters of the used device are summarized in Table II. The simulated input/output characteristics of MuMIC power amplifier by the harmonic balance method is shown in Fig. 3. As this figure indicates, this power amplifier is designed to have the gain of 34.5 dB for linear operation and the saturated power of 25.8 dBm.

IV. MuMIC DESIGN

We consider the multilayer MCM structure, i.e., multilayer microwave integrated circuits (MuMIC) to be the most effective candidate for the high frequency circuits. Fig. 4 shows the concept of the MuMIC structure. The conventional MMIC type power amplifier is shown in the left side, and the MuMIC power amplifier is shown in the other side. As is seen in this figure, conventional one's have huge size GaAs chips. That is due to every elements placed on GaAs chip. On the contrary, our MuMIC has the feature that circuit elements except for FET's are placed on multilayer structure of ceramic substrate. As a result, the GaAs chip size is reduced to be 10%. Further, total volume of MuMIC can be reduced to be smaller than that of MMIC. Because MuMIC has packageless and leadless features.

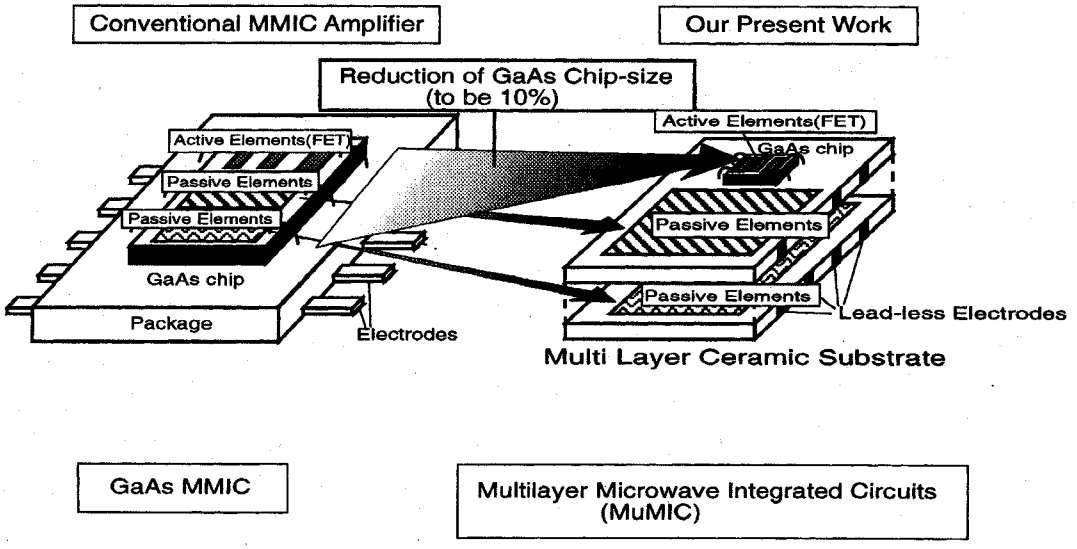


Fig. 4. Reduction of GaAs chip size.

TABLE III
RESISTANCE OF $\lambda/4$ LINE AND POWER ADDED EFFICIENCY

	Conventional MMIC Amplifiers	Our Present Work
Position	GaAs-Chip	MuMIC Substrate
Resistance	10 Ω	0.2 Ω
Efficiency	30%	40%
Structure	w=10mm t=3mm Au-Llines; GaAs MMIC; MuMIC w=200mm t=18mm Cu-Lines; Low fireing temprature ceramic substrate	

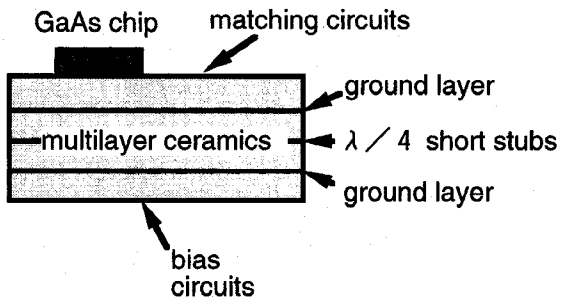


Fig. 5. Structure of MuMIC.

The structure of the newly developed MuMIC is shown in Fig. 5.

The MuMIC has three structural features as follows: First, matching circuits are formed on the surface of the MuMIC. Second, the $\lambda/4$ short stubs providing the bias circuits which occupy large circuits area are inserted in the third layer of the multilayer structure in order to reduce the size of the MuMIC. These circuits are sandwiched by ground layers in order to avoid coupling effects. Third, the low firing temperature multilayer ceramics are adopted as the substrate. Therefore, these stubs in bias circuits have the very low resistance in comparison with one's on GaAs chips, because the Cu metal lines with the 200-μm width and the 18-μm height are adopted as the strip lines. As a result, the 0.19 Ω resistance which generates only 0.02 V voltage down for the drain bias voltage is achieved for the $\lambda/4$ short stub. Therefore, it makes power added efficiency increase to over 40%, as shown in Table III.

The $\lambda/4$ short stub is designed by the computer aided design. Fig. 6(a) shows the simulated characteristics of the $\lambda/4$ short stub without coupling effects for the stub model of Fig. 6(b). However, the four-stage MuMIC amplifier contains four $\lambda/4$ short stubs. Therefore, the coupling effect becomes a serious factor to limit the quality of circuit with the increase of the integration density. The analysis of the coupling effect is carried out by the electromagnetic analysis of the moment method. The coupling characteristics are simulated by the way of the coupler model of two parallel oriented transmission lines with a quarter length of the propagating wavelength.

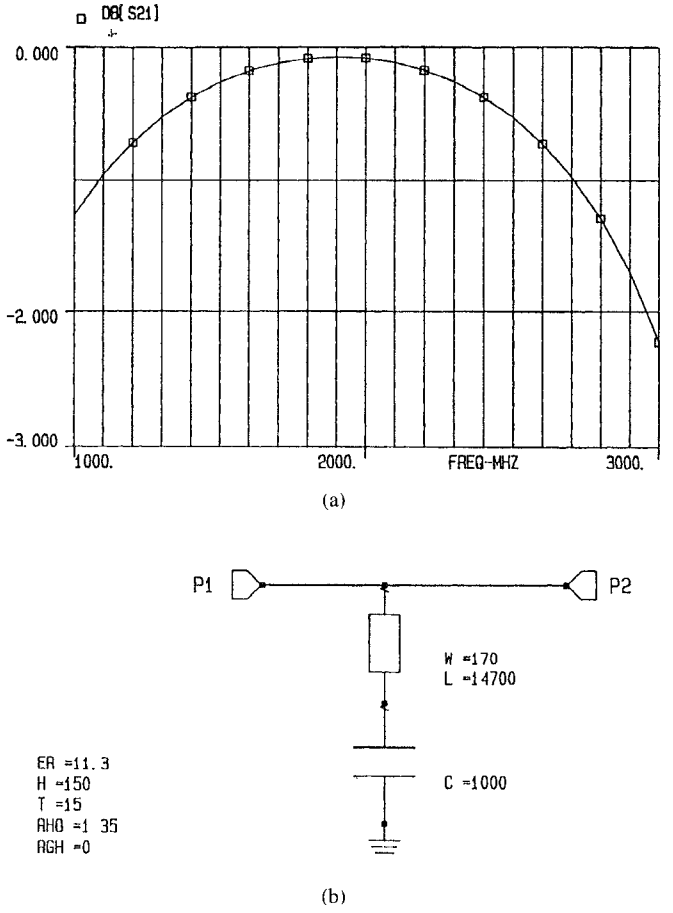


Fig. 6. $\lambda/4$ short stub characteristics.

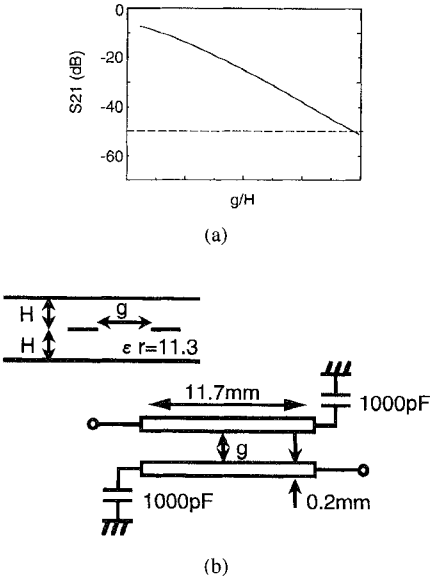


Fig. 7. $\lambda/4$ coupling characteristics.

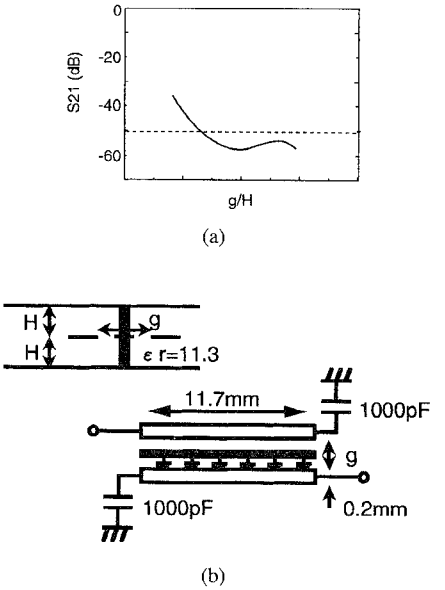


Fig. 8. $\lambda/4$ coupling characteristics with grounded line.

Fig. 7(a) shows the numerical result of the cross talk power characteristics for the coupling model of Fig. 7(b). In this figure, the normalized gap g/H which is the distance between the inner edges of the two strip lines with layer height H, having the value of bigger than about 4, provides the cross-talk power lower than -50 dB that is small enough for practical use. However, the g/H value of 4 means too large circuit area. Therefore, the grounded line is designed to be inserted between the two parallel transmission lines as shown in Fig. 8(b). Fig. 8(a) shows the numerical result for the design with the grounded line of Fig. 8(b). At this point of view, the condition with the grounded line is to be expected to have a lower cross-talk power than the condition without one. Therefore, the g/H value with the grounded line is designed to be as small as than 1.5.

Next, we design the via hole structure. The via hole characteristics are estimated by the simple model of Fig. 9(a) where the diameter and the height of the via hole are 100 μm and 150 μm, respectively. Fig. 9(b) shows S_{21}characteristics of the via hole. The insertion loss is estimated to be -0.03 dB for one via hole at 1.9 GHz.

The thermal analysis of the MuMIC is worth a mention in passing. The MuMIC thermal analysis model is shown in Fig. 10. The result of the calculation is that the thermal resistance is 128°C/W. Junction temperature is estimated to be 59.1°C which is obtained from considering the distortion power of 0.27 W for the ambient temperature of 25°C without the duty operation.

V. Fabrication

We used a full ion-implantation process to fabricate the GaAs chips. The BST capacitors on the GaAs chip were formed by using a simple sole-gel technique (7). Organic-based BST solution was spin-coated over Ti/Pt electrode followed by the annealing at 700°C. The uniformity of the fabricated capacitors had the variation less than 5%. The fabricated BST capacitor showed the very small temperature coefficient of less than 500 ppm/°C.

The photomicrographs of the present GaAs MMIC chip set are shown in Fig. 11(a) and (b). The size of these chips measures 550 μm $\times$ 1,010 μm and 600 μm $\times$ 900 μm, respectively. The total chip area of these GaAs chip sets is

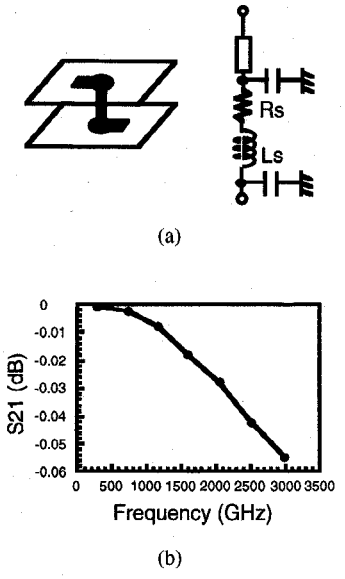


Fig. 9. Via hole model and simulated data.

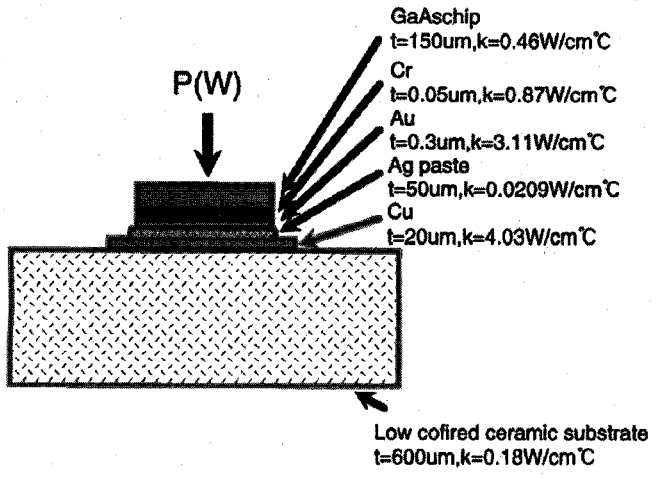


Fig. 10. MuMIC thermal analysis model.

reduced to be 1.1 mm^2 which is miniaturized by about 90% in comparison with usual reported one including the input/output matching circuits (6).

The photograph of the MuMIC with mounted GaAs MMIC's is shown in Fig. 12. The MuMIC measures 7.5 mm × 8 mm. The RF components such as chip capacitors were mounted on the surface of the MuMIC. The resistors for the bias circuits were prepared on the backside face layer of the MuMIC.

VI. RF Characteristics

The measured input/output characteristics is shown in Fig. 13. No additional matching circuit is used for 50- Ω measurement set-up. The saturation power was measured to be 24.3 dBm with power-added efficiency of 51% at the drain supply voltage of 3.6 V in 1.9 GHz frequency band. The 40.2% power-added efficiency has been obtained at the $P_{1\,\mathrm{dB}}$ of 22.2 dBm with the drain supply voltage of 3.6 V. A remarkable high gain as high as 35.8 dB with the $P_{1\,\mathrm{dB}}$ of 22.2 dBm has been provided with the −54 dBc adjacent channel distortion

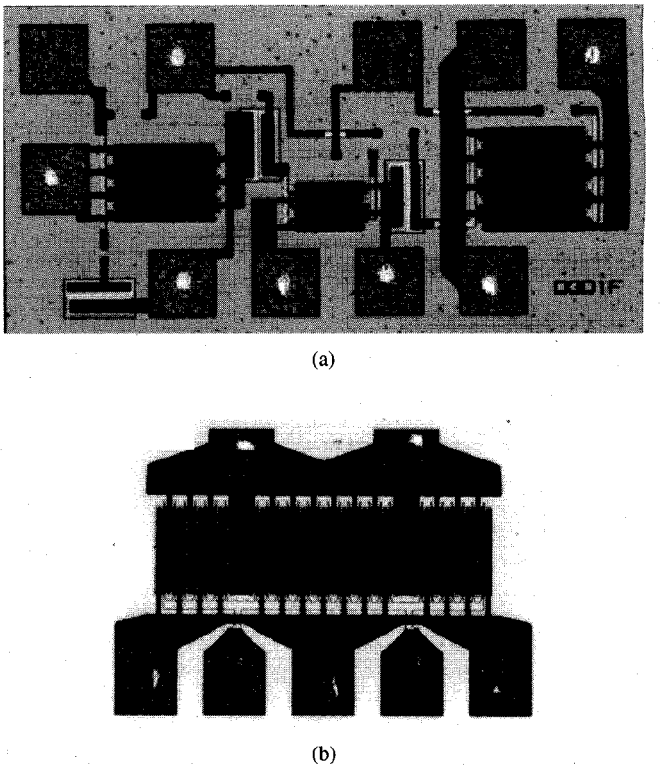


Fig. 11. Photomicrographs of the present GaAs MMIC chip set.

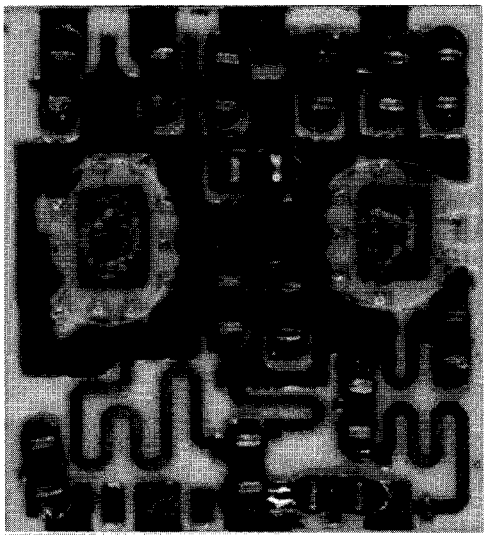


Fig. 12. Photomicrographs of MuMIC with mounted GaAs MMIC's.

at ±600 kHz for the $\pi/4$-shift QPSK modulation. Fig. 14 shows the output envelope of the power amplifier when tested at rated power using a nine bit pseudo-random code driving the $\pi/4$-shift QPSK modulated source.

It follows from what has been said that the MuMIC is increasing efficiency at low drain voltage and reducing chip area. One can safely state that the MuMIC is the most effective candidate for the high frequency circuits.

VII. Conclusion

A high efficiency GaAs MuMIC power amplifier for 1.9 GHz digital cordless telephones is demonstrated. The LDD

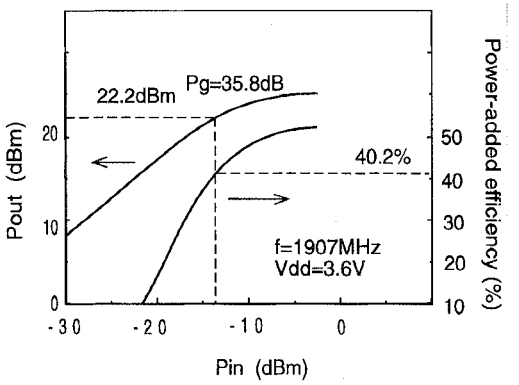
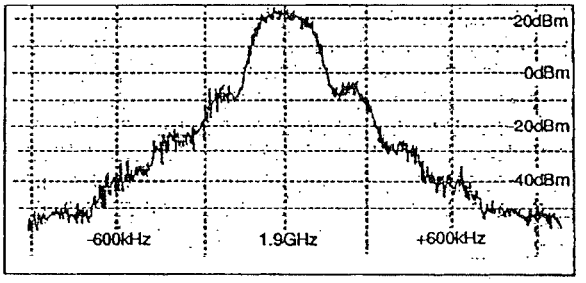


Fig. 13. Measured input–output characteristics of MuMIC power amplifier.



CENTER FREQUENCY	1.907GHZ
FREQUENCY SPAN	2MHz
RESOLUTION BANDWIDTH	30kHz
BIT RATE	384kbps/s

Fig. 14. Output envelope of the power amplifier under the tested condition at rated power using a nine bit pseudo-random code driving the $\lambda/4$-shift QPSK modulated source.

structure and the short gate length contributed to increasing the efficiency. The MuMIC structure and on-chip ferroelectric capacitors are employed to reduce the GaAs total chip area to be 1.1 mm^2 which is miniaturized by about 90% in comparison with usual one. The 40.2% efficiency and 35.8 dB gain at the $P_{1\,dB}$ of 22.2 dBm have been obtained with the -54 dBc adjacent channel distortion at ± 600 kHz for the $\pi/4$-shift QPSK modulation. We consider that the MuMIC is the most effective candidate for the high frequency circuits.

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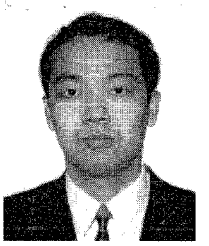

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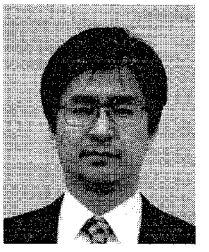

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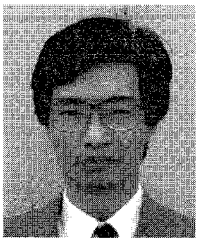

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